What is claimed is:

1. A semiconductor device for performing an N-bit prefetch operation, N being a positive integer, comprising:

a data strobe buffering means for generating N number of align control signals based on a data strobe signal and a external clock signal;

a receiving block in response to N-1 number of the align control signals for receiving N-bit data and outputting the N-bit data in a parallel fashion; and

a outputting block in response to the remaining align control signal for receiving the N-bit data in the parallel fashion and synchronizing the N-bit data with the remaining align control signal having a N/2 external clock period to thereby generating the synchronized N-bit data as a prefetched data.

2. The semiconductor device as recited in claim 1, wherein the data strobe buffering means generates the N number of align control signals, each having a N/2 external clock period.

3. The semiconductor device as recited in claim 2, wherein the receiving block includes N-1 number of latch blocks in response to the N-1 number of the align control signals.

4. The semiconductor device as recited in claim 3, wherein N is 4.

5. The semiconductor device as recited in claim 4, wherein the receiving block includes:

a first latching block for receiving 2-bit data and synchronizing the 2-bit data with a first align control signal to thereby generating the synchronized 2-bit data as a first synchronized data;

a second latching block for receiving the first synchronized data and synchronizing the first synchronized data with a second align control signal to thereby generating the synchronized 2-bit data as some of the N-bit data; and

a third latching block for receiving 2-bit data and synchronizing the 2-bit data with a third align control signal to thereby generating the synchronized 2-bit data as the other of the N-bit data.

6. The semiconductor device as recited in claim 4, wherein each of the first to third latching blocks includes at least one latch for synchronizing 1-bit data with one of the align control signals.

7. The semiconductor device as recited in claim 4, wherein the data strobe buffering means includes:

an instruction decoder for generating an initialization pulse in response to the data strobe signal; and

a strobe signal divider for receiving the data strobe signal and generating N number of the align control signals based on the strobe signal sequence,

wherein the strobe signal divider is initialized by the initialization pulse.

8. The semiconductor device as recited in claim 7, wherein the strobe signal divider includes:

first to forth strobe pulse generators, each for receiving the data strobe signal and generating the align control signals based on the strobe signal sequence; and

an initial setting block for initializing the first to forth strobe pulse generators,

wherein the align control signal has the N/2 external clock period.

9. The semiconductor device as recited in claim 7, wherein the data strobe buffering means includes a latency shifter coupled between the instruction decoder and the strobe signal divider for delaying the initialization pulse for a predetermined time.

10. The semiconductor device as recited in claim 7, wherein the data strobe buffering means includes a strobe signal buffer for receiving the data strobe signal and outputting data strobe signal to the strobe signal divider.

11. The semiconductor device as recited in claim 1, wherein the data strobe buffering means generates the N number of align control signals, at least one having a N/2 external clock period.

12. The semiconductor device as recited in claim 11, wherein the receiving block includes N-1 number of latch blocks in response to the N-1 number of the align control signals.

13. The semiconductor device as recited in claim 12, wherein N is 4.

14. The semiconductor device as recited in claim 13, wherein the receiving block includes:

a first latching block for receiving 2-bit data and synchronizing the 2-bit data with a first align control signal to thereby generating the synchronized 2-bit data as a first synchronized data;

a second latching block for receiving the first synchronized data and synchronizing the first synchronized data with a second align control signal to thereby generating the synchronized 2-bit data as some of the N-bit data; and

a third latching block for receiving the synchronized 2-bit data outputted from the second latching block and synchronizing the 2-bit data with a third align control signal to thereby generating the synchronized 2-bit data as the other

of the N-bit data.

15. The semiconductor device as recited in claim 14, wherein each of the first to third latching blocks includes at least one latch for synchronizing 1-bit data with one of the align control signals.

16. The semiconductor device as recited in claim 15, wherein N is 4.

17. The semiconductor device as recited in claim 13, wherein the data strobe buffering means includes:

an instruction decoder for generating an initialization pulse in response to the data strobe signal; and

a strobe signal divider for receiving the data strobe signal and generating N number of the align control signals based on the strobe signal sequence,

wherein the strobe signal divider is initialized by the initialization pulse.

18. The semiconductor device as recited in claim 17, wherein the strobe signal divider includes:

first to forth strobe pulse generators, each for receiving the data strobe signal and generating the align control signals based on the strobe signal sequence; and

an initial setting block for initializing the first to forth strobe pulse generators,

wherein the align control signal has the N/2 external clock period.

19. The semiconductor device as recited in claim 17, wherein the data strobe buffering means includes a latency shifter coupled between the instruction decoder and the strobe signal divider for delaying the initialization pulse for a predetermined time.

20. The semiconductor device as recited in claim 17, wherein the data strobe buffering means includes a strobe signal buffer for receiving the data strobe signal and outputting data strobe signal to the strobe signal divider.

21. The semiconductor device as recited in claim 1, wherein the outputting block includes N number of latches, each for synchronizing the N-bit data with the remaining align control signal having the N/2 external clock period to generate the synchronized N-bit data as the prefetched data.

22. The semiconductor device as recited in claim 1, further comprising: a global input-output driver for generating the prefetched data in response to the strobe enable signal.